REMARKS

Claims 1-21 are pending in the application.

Claims 1-21 were rejected.

Claims 1-21 were rejected under 35 U.S.C. 112.

Claims 1-21 were rejected under 35 U.S.C. 102(b).

Examiner Interview

Applicant thanks the Examiner for his time during the telephone interview on March 22, 2006. Applicant's representative, Brian Wichner, Reg. No. 52359, discussed this case with the Examiner.

The Examiner said that he has reviewed the case and realizes some aspects not realized before regarding the 112 rejection of claim 1. In this light, he also realizes that claim 5 appears allowable. The Examiner stated that he is removing the 112 rejection of claim 1, and conditionally allowing claim 5 under objection as being dependent upon a rejected claim. He will send an Examiner Interview Summary.

Claim Amendments

Claims 1, 6, and 15 have been amended, but only to include a previously depending claim 5. No new matter, and no substantively different material, has been added. No new search is necessitated by this amendment.

Claim 11 has been amended to overcome a section 112 rejection.

Claim Rejections – 35 U.S.C. § 112

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant respectfully traverses the rejection.

Claim 1 recites switches responsive to a *control signal*, and a boosting voltage configured to vary according to a logic state of a *boosting level control signal.*

The are two separate and distinct signals. The signal IN is a third separate and distinct signal.

The examiner has indicated that claim 1 recites or implies that SW1 and SW2 are responsive to signal IN. This is not true, however, and the Specification does not teach this..

Instead, SW1 and SW2 are responsive to a control signal that is not explicitly shown in the figures. The control signal is supported in the Specification on page 2, lines 21-22. One of ordinary skill in the art would consider such a control signal for switches to be common knowledge, so switch control signals are not shown in the figures.

The signal IN, in the embodiment of FIG. 1, acts as an input clock signal for the boosting level control signal BCON.

Regarding claim 6, support is readily found in the Specification on page 3, lines 17-21. Here, the first state is the BCON signal is "low". Then the output of the NOR gate, which is the driving node N1, will be "high" when inverted (from inverter I2) IN clocks "low" also. This will result in a relatively increased boosting voltage. Otherwise, with a second logic state, "high", the driving node will be fixed at the ground level, resulting in a relatively decreased boosting voltage. These two cases are also summarized on page 4, lines 5-12.

The Examiner notes that FIGS. 2 and 3 show an "increasing" step occurring after time t1. The claim doesn't exclude this, but claim 6 does recite conditions for either increasing or decreasing a boosting voltage. And this is all supported by the Specification, as explained above.

Claim 11 has been amended to recite that the logic device is a NOR gate. Claim 11 no longer claims *an additional* logic gate.

Regarding claim 15, first and second control signals are independent and distinct, as explained above. Specifically, first control signal controls SW1 and SW2. The first control signal is not explicitly shown in the figures, but is supported in the Specification on page 2, lines 21-22. One of ordinary skill in the art would consider such a control signal for switches to be common knowledge, so switch control signals are not shown in the figures. Separately, the second control signal recited in claim 15 is supported in the embodiment of FIG. 1 as the BCON signal input to the NOR gate O1. Both first and second signals operate independently of each other.

Applicant requests withdrawal of the rejection for these claims.

Claim Rejections – 35 U.S.C. § 102

Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Soneda, et al. (5,856,918).

Applicant respectfully traverses the rejection.

Claims 1 and 15 have been amended to include the limitations of claim 5, and no other limitations have been added. No new search is necessary. Claims 1 and 15 now recite,

among other things, switches responsive to a control signal, a boosting voltage configured to vary in response to a boosting level control signal, and a logic device having an input to receive the boosting level control signal, wherein the control signal and the boosting level control signal are configured to operate independently of each other, and an external supply voltage detector configured to detect the external supply voltage level and to generate the boosting level control signal.

Soneda does not teach these limitations of claims 1 and 15. For example, the Examiner notes that Soneda shows, in FIG. 2, a driving node K1, boosting capacitors C1-C3, switches PT2 and PT3, a control signal CLK3, a boosting level control signal CLK1, an external supply voltage detector NU1, NU2, or NU3, and a logic gate PT1 and/or NL1. But claim 1 recites that the external supply voltage detector is configured to generate the boosting level control signal. NU1, NU2, or NU3, cannot be an external supply voltage detector because they do not have any connection to an input of a logic device to receive the boosting level control signal, as recited in claim 1. The examiner notes that the logic device is either PT1 and/or NL1. And neither NU1, NU2, nor NU3 is connected to PT1 and/or NL1. Thus, all the limitations of claims 1 and 15 are not anticipated by Soneda.

Claim 6 has been amended to include the limitations of claim 5, and no other limitations have been added. No new search is necessary. Claim 6 now recites, among other things, detecting an external supply voltage level using an external supply voltage detector, and generating the boosting level control signal as an output of the external supply voltage detector. Soneda fails to anticipate the recited method as explained above regarding claims 1 and 15.

For the foregoing reasons, reconsideration and allowance of claims 1-21 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,
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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on March 30, 2006.

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